

# Exhibit 14



Paper No. 26

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

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IPR2022-00999

Patent 11,232,054 B2

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**PETITIONER'S REPLY  
TO PATENT OWNER'S RESPONSE**

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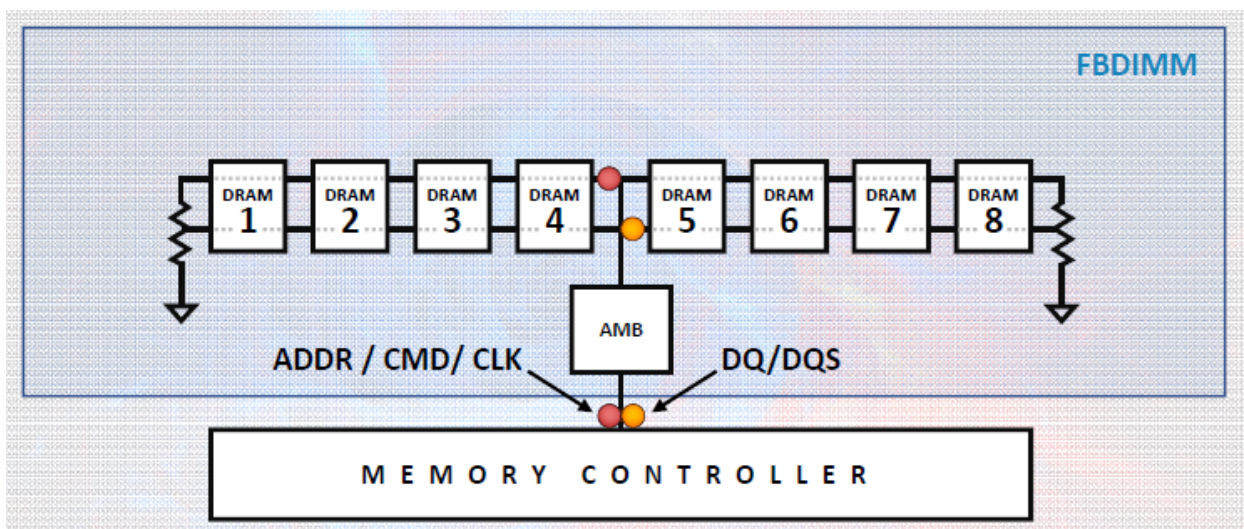
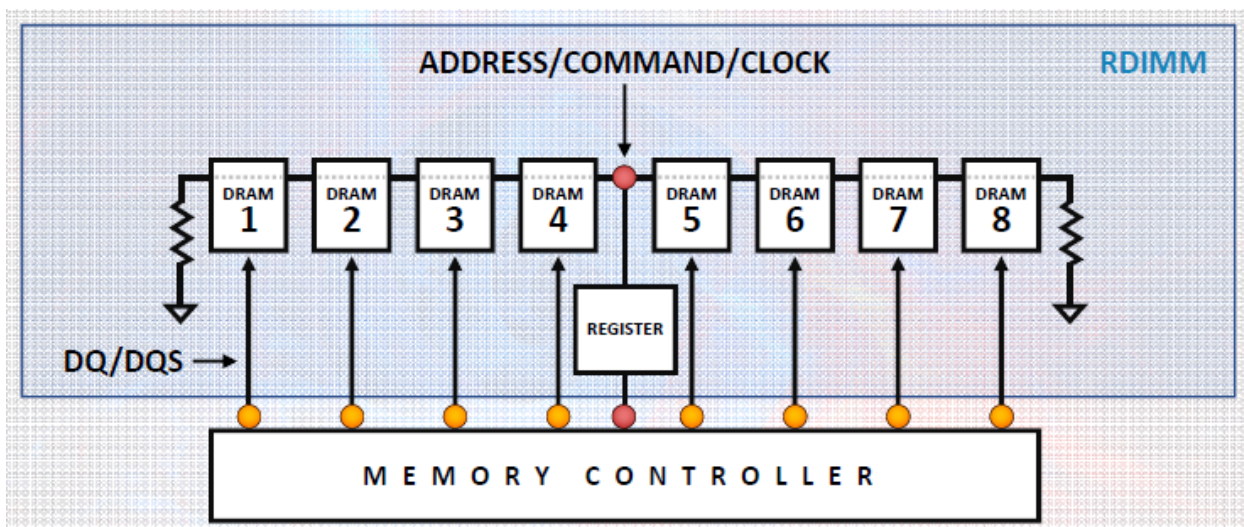
consistent with the combination for Grounds 2-3: the side connection could be used for battery backup (as taught by Amidi), and the edge connections could be used for power from the host system during normal operation (as taught by Harris):



EX2035, 39; EX1075, 165:10-166:12.

**2. Harris discloses receiving “*data, address, and control signals*” from the host (POR 14-18)**

As shown below by Netlist’s technology tutorial, an FBDIMM (second below) receives *signals* for data (DQ), address (ADDR), and control (CMD), similar to an RDIMM memory module (first below):



EX1077, 8-9; EX1075, 91:23-92:19, 95:14-96:13, 97:16-98:18.

Netlist incorrectly argues that Harris's FBDIMM (or FBD) does *not* receive data, address, and control "signals" from the host system because, under the FBDIMM standard, those signals are *encoded* first into a packetized signal that can be sent to the AMB (shown above) on fewer wires than if the signals were all sent separately. POR 14; EX2061, ¶31; EX1075, 155:22-157:1; EX2060, 8:3-11:6. In essence, Netlist is trying to rewrite the claims (and its expert's testimony) to

require “*dedicated* pins” for address, command, and data, EX1075, 212:3-:8, 213:3-215:20, 219:13-220:9, 226:7-228:8, even though that is not what the claims say, and the specification specifically identifies FBDIMM as an embodiment of the invention. EX1001, 21:46-:55 (“fully-buffered (FBDIMM)”). Excluding a preferred embodiment from the claims is “rarely, if ever correct.” *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022).

Indeed, Netlist concedes that the signals received by the AMB on the FBDIMM *result* in “data, address, and control *signals* needed by the DDR2 SDRAMs.” EX2061, ¶31. And the FBDIMM standard confirms that “[a]ll memory control for the DRAM *resides in the host*, including *memory request initiation*,” and the AMB “[a]cts as DRAM memory buffer for all *read, write*, and configuration accesses addressed to the DIMM.” EX1027, p.1. As a buffer for all such commands to the FBDIMM, the AMB must necessarily couple data, address, and control *signals* from the host system to the memory module—exactly like the claims require.

3. **Harris and the FBDIMM Standards render obvious using *three* buck converters (POR 18-33)**

The Board correctly rejected Netlist’s argument, repeated here, that it was not obvious to use *three* buck converters. ID 21-23.